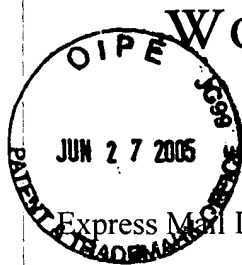


RICK D. NYDEGGER  
BRENT P. LORIMER  
THOMAS R. VUKSINICK  
LARRY R. LAYCOCK  
JONATHAN W. RICHARDS  
DAVID R. WRIGHT  
JOHN C. STRINGHAM  
JOHN M. GUYNN  
CHARLES L. ROBERTS  
DANA L. TANGREN  
ERIC L. MASCHOFF  
CHARLES J. VEVERKA  
ROBYN L. PHILLIPS  
RICHARD C. GILMORE \*  
STERLING A. BRENNAN  
R. BURNS ISRAELSEN  
DAVID R. TODD  
DAVID B. DELLENBACH  
L. DAVID GRIFFIN  
ADRIAN J. LEE  
FRASER D. ROY  
CARL T. REED



R. PARRISH FREEMAN, JR.  
PETER F. MALEN, JR.  
L. REX SEARS, PH.D.  
WILLIAM R. RICHTER  
ERIC M. KAMERATH  
ROBERT E. AYCOCK  
JENS C. JENKINS  
MICHAEL B. DODD  
KEVIN W. STINGER  
WILLIAM J. ATHAY  
RYAN D. BENSON  
SARA D. JONES  
TIGE KELLER  
JANNA L. JENSEN  
MATTHEW D. TODD  
J. LAVAR OLDHAM  
MICHAEL J. FRODSHAM  
JOSEPH L. KRUPA  
BRETT A. HANSEN  
BRETT I. JOHNSON  
MATTHEW A. BARLOW  
WESLEY C. ROSANDER  
ANDREW S. HANSEN  
CHAD E. NYDEGGER  
JOSEPH G. PIA  
CLINTON E. DUKE  
RYAN N. FARR \*  
JAMES B. BELSHE  
KIRK R. HARRIS  
KEELY SCHNEITER  
MICHAEL M. BALLARD  
DAVID A. JONES  
SHANE K. JENSEN  
JONATHAN M. BENNS, PH.D.

VERNON R. RICE §  
OF COUNSEL



# WORKMAN | NYDEGGER

INTELLECTUAL PROPERTY ATTORNEYS

1000 EAGLE GATE TOWER  
60 EAST SOUTH TEMPLE  
SALT LAKE CITY, UTAH 84111  
TELEPHONE: (801) 533-9800  
FAX: (801) 328-1707  
WEBSITE: HTTP://WWW.WNLAW.COM

Express Mail Label No. EV 566 183 400 US

PATENT APPLICATION  
Docket No.: 14321.63

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: )  
)  
Toshiki Makimoto, et al. )  
)  
Serial No.: 10/516,380 ) Art Unit  
) 2811  
Filed: November 30, 2004 )  
)  
Confirmation No.: 2860 )  
)  
For: P-TYPE NITRIDE SEMICONDUCTOR )  
STRUCTURE AND BIPOLAR TRANSISTOR )

### TRANSMITTAL FOR INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing and pursuant to 37 C.F.R. § 1.97 is an Information Disclosure Statement, which includes the following statements, if any, required variously by 37 C.F.R. § 1.98:

- ☒ Statement of relevance of selected cited references not in the English language which are not translated.
- ☐ Statement that selected cited references are substantially cumulative of an enclosed or previously submitted reference.
- ☐ Statement that selected cited references were previously cited by or submitted to the United States Patent and Trademark Office in a prior application which is relied upon for an earlier filing date under 35 U.S.C. § 120.

A. Additional Materials Required Due to Content of Information Disclosure Statement

Transmitted are the following documents in addition to the Information Disclosure Statement as required variously under 37 C.F.R. § 1.98:

- ☒ Form PTO-1449 listing 18 references submitted for consideration.
- ☒ A copy of 17 Non-US references listed on the Form PTO-1449.
- ☐ English translations of \_\_\_ (\_\_\_) of the references listed on the Form PTO-1449 which are not in the English language.
- ☐ Copies of the following documents from the prosecution of a previous, related application:
  - ☐ Form PTO-1449 AND INFORMATION DISCLOSURE STATEMENT; and
  - ☐ Form PTO-892

B. Additional Materials Required Due to Timing of Filing of Information Disclosure Statement

The transmitted Information Disclosure Statement is being filed within one (1) of the following four (4) time periods:

- ☒ Prior to the later of either three (3) months following the filing date or the mailing of a first Office Action. Accordingly, no materials other than those listed above are enclosed.
- II. ☐ Following the latter of either three (3) months following the filing date or the mailing of a first Office Action, but before the mailing of a final Office Action or a Notice of Allowance. Accordingly, to secure consideration thereof, one (1) of the following is also enclosed:
  - ☐ Promptness Certification; or
  - ☐ Check No. \_\_\_\_\_ in the amount of \_\_\_ constituting the submission fee set forth in 37 C.F.R. § 1.17(p).
- III. ☐ After the mailing of a Notice of Allowance, but before payment of the Issue Fee. Accordingly, in order to secure consideration thereof, each of the following are also enclosed:
  - ☐ Promptness Certificate;
  - ☐ Petition for Consideration; and
  - ☐ Check No. in the amount of \_\_\_ constituting the petition fee set forth in 37 C.F.R. § 1.17(i)(1).

IV. \_\_\_\_\_ After payment of the Issue Fee. Accordingly, in order to secure consideration thereof, each of the following are also enclosed:

\_\_\_\_\_ Petition to Withdraw from Issue; and

\_\_\_\_\_ Check No. \_\_\_\_\_ in the amount of \_\_\_\_\_ constituting the petition fee set forth in 37 C.F.R. § 1.17(i)(1).

C. Fees

The Commissioner is hereby authorized to charge payment of or any deficiency in the following fees associated with this communication, or to credit any overpayment thereof, to Deposit Account No. 23-3178. A duplicate copy of this letter is enclosed.

X Any fee required in relation to filing of this letter or any documents transmitted therewith.

\_\_\_\_\_ The submission fee set forth in 37 C.F.R. § 1.17(p) in the event that 37 C.F.R. § 1.97(c) applies and the Examiner is not satisfied that any Promptness Certificate submitted meets the requirements of 37 C.F.R. § 1.97(e).

\_\_\_\_\_ The submission fee set forth in 37 C.F.R. § 1.17(p).

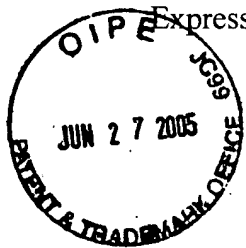
\_\_\_\_\_ The petition fee set forth in 37 C.F.R. § 1.17(i)(1).

Dated this 27<sup>th</sup> day of June 2005.

Respectfully submitted,



DANA L. TANGREN  
Attorney for Applicant  
Registration No. 37,246  
Customer No. 022913  
Telephone No. 801.533.9800



Express Mail Label No. EV 566 183 400 US

PATENT APPLICATION

Docket No.: 14321.63

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Toshiki Makimoto, et al.

Serial No.: 10/516,380

Filed: November 30, 2004

Confirmation No.: 2860

For: P-TYPE NITRIDE SEMICONDUCTOR  
STRUCTURE AND BIPOLAR TRANSISTOR

)  
)  
)  
)  
) Art Unit  
) 2811  
)  
)  
)  
)  
)  
)

INFORMATION DISCLOSURE STATEMENT  
UNDER 37 C.F.R. § 1.97

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Please find, pursuant to 37 C.F.R. § 1.98(a)(1), the enclosed Form PTO-1449 which contains a list of all patents, publications, or other items that have come to the attention of one or more of the individuals designated in 37 C.F.R. § 1.56(c). While no representation is made that any of these references may be "prior art" within the meaning of that term under 35 U.S.C. §§ 102 or 103, the enclosed list of references is disclosed so as to fully comply with the duty of disclosure set forth in 37 C.F.R. § 1.56.

Moreover, while no representation is made that a specific search of office files or patent office records has been conducted or that no better art exists, the undersigned attorney of record

believes that the enclosed art is the closest to the claimed invention (taken in its entirety) of which the undersigned is presently aware, and no art which is closer to the claimed invention (taken in its entirety) has been knowingly withheld.

In accordance with 37 C.F.R. §§ 1.97 and 1.98, a copy of each of the listed non U.S. Patent references or relevant portion thereof is also enclosed.

Statement of Relevance of References Listed  
Unaccompanied by English Translation  
Under 37 C.F.R. § 1.98(a)(3)

In accordance with 37 C.F.R. § 1.98(a)(3), the following concise explanation of the relevance of each listed reference that is not in the English language and unaccompanied by a translation into English is provided.

Japanese Publication No. 05-175225: PURPOSE: To obtain a manufacturing method of an HBT of collector-up structure wherein a base resistance and a base-emitter junction capacitance are reduced or an HBT of emitter-up structure wherein a base resistance and a base-collector capacitance are reduced. CONSTITUTION: An NPN type HBT of collector-up structure consists of a semiconductor layer containing the following; an N-type AlGaAs emitter layer 3 on a GaAs substrate 1, a P-type GaAs base layer 4 which is formed on the layer 3 and has a band gap narrower than that of the layer 3, and an N-type GaAs collector layer 5 formed on the layer 4. When the above HBT is manufactured, a high resistance region 9 is selectively constituted in the N-type AlGaAs emitter layer 3 by implanting oxygen ions while using a first insulating film and a second insulating film side wall as masks. By an epitaxial re-growth method using a mask, the collector-up type HBT is selectively deposited and manufactures so as to be in contact with only the outer emitter layer 9 so as to be in contact with only the outer emitter layer 9 where a P-type GaAs outer base layer 10 is made highly resistive and the base layer 4.

Japanese Publication No. 05-291282: PURPOSE: To reduce a parasitic leakage current to a satisfactory extent by selectively eliminating a second insulating film, exposing an outer base layer comprising a third semiconductor layer and forming a base electrode in a self-alignment fashion and enhance high frequency properties, and especially a maximum oscillation frequency by further reducing base resistance dramatically. CONSTITUTION: Formation of an outer emitter high resistor layer 7 stabilized by oxygen ion implantation reduces a parasitic leakage current flowing during the junction of an outer emitter base. Moreover, the base resistance is reduced by connecting continuously a high concentration outer base layer 8 and a collector layer 10 to an inner intrinsic base layer 4 and making an epitaxial growth based on a regrowth process and forming a base electrode 14 in a self-alignment fashion. This construction

makes it possible to reduce the base resistance dramatically and enhance a current amplification factor, high frequency properties and especially a maximum oscillation frequency.

Japanese Publication No. 07-245316: PURPOSE: To provide an HBT which is high in operating speed, low in power consumption, and has excellent element characteristics by reducing the thickness of an intrinsic base layer under high controllability and reducing the sheet resistance and contact resistance of an external base layer. CONSTITUTION: A p+-type GaAs intrinsic base layer 22, n-type Al<sub>0.25</sub>Ga<sub>0.75</sub>As emitter 24, etc., are successively formed on the central part of an n-type GaAs collector layer 14. In addition, a p+-type GaAs external base layer 18 is formed on the collector layer 14 around the base layer 22 with an n-type InGaP etching stopper layer 16 in between. The base layer 22, emitter layer 24, etc., etc., are regrown on the collector layer 14 exposed by selectively etching the base layer 18 by utilizing the etching stopper layer 16.

Japanese Publication No. 2003-007998: PROBLEM TO BE SOLVED: To provide a p-type nitride semiconductor structure having a high hole concentration and low resistance and to provide a method of manufacturing the structure. SOLUTION: The semiconductor structure is constituted of nitride semiconductors doped with a p-type impurity. In the structure, a semiconductor 1 having a lattice constant  $a_1$  and another semiconductor 2 having a different lattice constant  $a_2$  are joined together in a lattice strain containing state. More than 5% of the dopant contained in the semiconductor 1 is activated. The activating heat treatment for activating the dopant is performed at a temperature of  $\geq 600^\circ\text{C}$  in the joined state.

Japanese Publication No. 2002-305204: PROBLEM TO BE SOLVED: To realize a low-resistance nitride semiconductor structure, and to constitute a heterojunction bipolar transistor high in current gain, using the nitride semiconductor structure as a base layer. SOLUTION: In this heterojunction bipolar transistor, where a base layer constituted of an Mg-doped p-type InGa<sub>N</sub> is made between an emitter layer and a collector layer, In composition of that base layer is changed, according to the distance from that emitter layer to that base layer, and the depth of the acceptor level within that base layer is changed together with a band gap. Since holes are discharged at a high rate from the acceptor level, the resistance of that base layer drops, and a region where the positive poles are accumulated becomes an effective base layer; and since the width  $W_{\text{eff}}$  is smaller than the width  $W_b$  of the structural base layer, the current gain rises  $(W_b/W_{\text{eff}})^2$  times (this magnification is larger than 1).

Japanese Publication No. 10-065216: PROBLEM TO BE SOLVED: To decrease the ohmic resistance between a metal electrode and a III nitride semiconductor layer by setting the band gap of a contact layer, provided between the III nitride semiconductor layer and the metal electrode, to be lower than that of the III nitride semiconductor layer and specifying the thickness of the contact layer. SOLUTION: A buffer layer 2, a silicon-doped n-GaN layer 3, a lower class layer 4, a light emission layer 5 and an upper clad layer 6 are formed on a sapphire substrate 1. A contact layer 11 and a metal electrode 7 are formed on the upper clad layer 6 of a III nitride semiconductor ( $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ , including  $X=0, Y=0, X=Y=0$ ). The contact layer 11 is formed of the III nitride semiconductor ( $\text{Al}_s\text{In}_y\text{Ga}_{1-s-y}\text{N}$ , including  $X=0, Y=0, X=Y=0$ ), and the band gap thereof is set lower than that of the upper clad layer 6 and the thickness thereof is set in the range of 1-50nm.

Japanese Publication No. 11-150296: PROBLEM TO BE SOLVED: To prolong a service life of a nitride semiconductor element and improve the reliability of the element by improving the quality of a p-type conductive layer, which the cost of the element is reduced and the productivity of the element is improved by making a heat treatment after the growth unnecessary. SOLUTION: A nitride semiconductor laser is constituted, by successively forming an undoped GaN base layer 12, an n-type GaN contact layer 13, an n-type AlGaIn current injecting layer 14, a GaN light guide layer 15, an InGaIn active layer 16, a GaN optical guide layer 17, a p-type AlGaIn current injecting layer 18, a p-type GaN contact layer 19, and a p-side electrode 22 on a sapphire substrate 11. The surface oxygen concentration of the p-type GaN contact layer 19 is set to  $\leq 5 \times 10^{18} \text{ cm}^{-3}$ , and the maximum value of the oxygen concentration near the surface of the layer 19 is set to a quintuple of the in-surface average oxygen concentration of the layer 19 or lower.

Abstract of Article Entitled *High Current Gain of 3000 for GaN/InGaIn HBTs with A Regrown Base Layer*: GaN/InGaIn double heterojunction bipolar transistors with the regrown p-InGaIn extrinsic base have been fabricated on SiC substrates. The maximum common-emitter current gain exceeds 3000 at the collector current of 20 mA for the 50  $\mu\text{m}$  and 30  $\mu\text{m}$  device. Furthermore, the offset voltage in the common-emitter current-voltage characteristics has reduced from 5V to 1V. This result indicates that the large offset voltage reported previously is mainly ascribed to the degraded base ohmic characteristics. The regrowth of p-InGaIn is effective to improve the characteristics of nitride heterojunction bipolar transistors.

Dated this 27<sup>th</sup> day of June 2005.

Respectfully submitted,

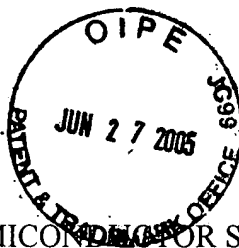


DANA L. TANGREN  
Attorney for Applicant  
Registration No. 37,246  
Customer No. 022913  
Telephone No. 801.533.9800

EMK:ahm  
AHM0000000513V001

Form PTO-1449

Applicant: Toshiki Makimoto, et al.  
 Serial No.: 10/516,380  
 Filing Date: November 30, 2004  
 For: P-TYPE NITRIDE SEMICONDUCTOR STRUCTURE AND BIPOLAR TRANSISTOR



Sheet 1 of 3  
 Confirmation No.: 2860  
 Att'y Docket No.: 14321.63  
 Art Unit: 2811

# INFORMATION DISCLOSURE CITATIONS MADE BY APPLICANT

## U.S. Patent Documents

<u>Examiner Initial*</u>	<u>Document Number</u>	<u>Issue Date</u>	<u>Name</u>
____ 1	2002/0146855 A1	10/10/2002	Goto et al.

## Foreign Patent Documents

<u>Examiner Initial*</u>	<u>Document Number</u>	<u>Publication Date</u>	<u>Country or Patent Office</u>	<u>Translation</u>
____ 2	5-175225	7/13/1993	Japan	No
____ 3	5-291282	11/5/1993	Japan	No
____ 4	7-245316	9/19/1995	Japan	No
____ 5	2003-007998	1/10/2003	Japan	No
____ 6	2002-305204	10/18/2002	Japan	No
____ 7	10-065216	03/06/2002	Japan	No
____ 8	11-150296	06/02/1999	Japan	No

## Other Documents

(including author, title, pertinent pages, etc.)

<u>Examiner Initial*</u>	
____ 9	K. Kumakura, T. Makimoto and N. Kobayashi, <i>Low-Resistance Nonalloyed Ohmic Contact to p-type GaN Using Strained InGaN Contact Layer</i> , Applied Physics Letters, Vol. 79, No. 16, pp 2588-2590 (2001).

Examiner:

Date Considered:

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



Applicant: Toshiki Makimoto, et al.

Confirmation No.: 2860

Serial No.: 10/516,380

Att'y Docket No.: 14321.63

Filing Date: November 30, 2004

Art Unit: 2811

For: P-TYPE NITRIDE SEMICONDUCTOR STRUCTURE AND BIPOLAR TRANSISTOR

- \_\_\_\_\_ 10 T. Makimoto, et al., *Reduced Damage Of Electron Cyclotron Resonance Etching By In Doping Into p-GaN*, Journal of Crystal Growth 221, pp. 350-355 (2000).
- \_\_\_\_\_ 11 T. Makimoto, et al., *High Current Gains Obtained by InGaN/GaN Double Heterojunction Bipolar Transistors*, phys. stat. sol. (a) 188, No. 1, pp. 183-186, (2001).
- \_\_\_\_\_ 12 L.S. McCarthy, et al., *AlGaIn/GaN Heterojunction Bipolar Transistor*, IEEE Electron Device Letters, Vol. 20, No. 6, pp. 277-270 (1999).
- \_\_\_\_\_ 13 B.S. Shelton, et al., *Selective Area Growth and Characterization of AlGaIn/GaN Heterojunction Bipolar Transistors by Metalorganic Chemical Vapor Deposition*, IEEE Transactions on Electron Devices, Vol. 48, No. 3, pp. 490-494 (2001).
- \_\_\_\_\_ 14 K.P. Lee, et al., *Self-Aligned Process for Emitter- and Base-Regrowth GaN HBTs and BJTs*, Solid-State Electronics 45, pp. 243-247 (2001),
- \_\_\_\_\_ 15 T. Makimoto et al., *High Current Gain of 3000 for GaN/InGaIn HBTs with a Regrown Base Layer*, Technical Report of IEICE. ED2003-25 CPM2003-24 SDM2003-25 (2003-5), pp. 49-52.
- \_\_\_\_\_ 16 T. Makimoto et al., *High Current Gain of 3000 for GaN/InGaIn Double Heterojunction Bipolar Transistors with Regrown p-InGaIn Extrinsic Base*, Technical Digest of 5<sup>th</sup> International Conference on Nitride Semiconductors, May 25-30, 2003, p. 195.
- \_\_\_\_\_ 17 T. Makimoto et al., *High Current Gain (>2000) and Reduced Common-emitter Offset Voltage of GaN/InGaIn Double Heterojunction Bipolar Transistors*, Conference Digest of 61<sup>st</sup> Device Research Conference, pp. 23-24, June 23-25, 2003.
- \_\_\_\_\_ 18 T. Makimoto et al., *High Current Gain (>2000) of GaN/InGaIn double Heterojunction Bipolar Transistors Using Base Regrowth of p-InGaIn*. Applied Physics Letters, Vol. 83, No. 5, pp. 1035-1037 (2003).

Examiner:

Date Considered:

Applicant: Toshiki Makimoto, et al.

Confirmation No.: 2860

Serial No.: 10/516,380

Att'y Docket No.: 14321.63

Filing Date: November 30, 2004

Art Unit: 2811

For: P-TYPE NITRIDE SEMICONDUCTOR STRUCTURE AND BIPOLAR TRANSISTOR

---

**References Cited by Applicants**

While the filing of Information Disclosure Statements is voluntary, the procedure is governed by the guidelines of Section 609 of the Manual of Patent Examining Procedure and 37 C.F.R. §§ 1.97 and 1.98. To be considered a proper Information Disclosure Statement, Form PTO-1449 shall be accompanied by a copy of each listed patent or publication or other item of information and a translation of the pertinent portions of foreign documents (if an existing translation is readily available to the applicant), an explanation of relevance of each reference not in the English language, and should be submitted in a timely manner as set out in MPEP Sec. 609.

Examiners will consider all citations submitted in conformance with 37 C.F.R. § 1.98 and MPEP Sec. 609 and place their initials adjacent the citations in the spaces provided on this form. Examiners will also initial citations not in conformance with the guidelines which may have been considered. A reference may be considered by the Examiner for any reason whether or not the citation is in full conformance with the guidelines. A line will be drawn through a citation if it is not in conformance with the guidelines AND has not been considered. A copy of the submitted form, as reviewed by the Examiner, will be returned to the applicant with the next communication. The original of the form will be entered into the application file.

Each citation initialed by the Examiner will be printed on the issued patent in the same manner as references cited by the Examiner on Form PTO-892.

The reference designations "A1," "A2," etc. (referring to Applicant's reference 1, Applicant's reference 2, etc.) will be used by the Examiner in the same manner as Examiner's reference designations "A," "B," "C," etc. on Office Action Form PTO-1142.

W:\14321\63\DFW0000014407V001.doc

---

Examiner:

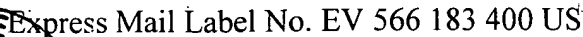
Date Considered:

---

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

---

Ifw/2811



Docket No.: 14321.63

In re application of:

Serial No.:

10/516,380

Filed:

November 30, 2004

Confirmation No.:

2860

For:

# P-TYPE NITRIDE SEMICONDUCTOR STRUCTURE AND BIPOLAR TRANSISTOR

I hereby certify that the following documents are being deposited with the United States Postal Service as Express Mail, postage prepaid, in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, Virginia 22313-1450 20231; on the 27<sup>th</sup> day of June 2005.

- Transmittal for Information Disclosure Statement (3 pages)
- Information Disclosure Statement (4 pages)
- Form PTO-1449 listing 18 references (2 pages)
- A copy of 17 Non-US listed reference
- Postcard

*Nam Tangren*

DANA L. TANGREN

Attorney for Applicant

Registration No. 37,246

Customer No. 022913

Telephone: (801) 533-9800

Facsimile: (801) 328-1707

DLT:dfw

W:\14321\63\AHM00000005\3V001.DOC